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Integrated Circuit
Application Note

CHOOSING DTL INTEGRATED LOGIC CIRCUITS

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This article discusses diode-transistor logic, DTL, integrated circuits, and the considerations a user should make in choosing this IC family. Consideration is given to the advantages and limitations one encounters with this logic form. Three versions of DTL are considered in this report; conventional DTL, modified DTL, and high noise immunity DTL.

MOTOROLA Semiconductor Products Inc.

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INTRODUCTION

With the wide variety of integrated circuits on the market today--RTL, DTL, T^2L, etc.--one often hears the question "how does one who is using integrated circuits for the first time go about selecting a logic line suitable to meet his requirements?" Certainly, no one family of ICs can satisfy the demands of all logic designers, nor meet completely all the specifications of a given digital system. However the many different logic types available today permit selection of one that comes close to satisfying most requirements. Consequently, the problem becomes one of assembling sufficient information about all logic types to make possible a decision.

One important point should be emphasized. With the increasing competition in the electronic marketplace, those who are not now at least considering the design of their equipment using ICs might soon find themselves in a serious non-competitive position. In view of the decision facing many semiconductor users on whether or not to go with ICs, Motorola IC Applications Engineering has prepared a series of notes, each one dealing with the significant factors to consider in choosing a particular IC line.

The purpose of this report is to present the significant facts about the use of diode-transistor logic (DTL). No attempt is made at listing details for design with this logic. The objective is to present those factors that would be of initial interest in considering DTL versus RTL, MECL, T^2L, etc. Full consideration is given to the advantages as well as the limitations one encounters in using DTL.

This report further considers the three versions of DTL: conventional two-diode offset type; the recent modified version; and, finally, high noise immunity DTL. Basic circuit configurations are discussed, and some of the important characteristics are mentioned.

Similar papers have been prepared to present those considerations that are appropriate in choosing integrated resistor-transistor (RTL) and high speed emitter-coupled logic (ECL) and transistor-transistor logic (T^2L). Consult the "Application Note Index", for the appropriate application note numbers.

DIODE – TRANSISTOR LOGIC

A logic circuit form that was very familiar to the discrete designer was one that used diodes and transistors as the main components. The diodes provided higher signal thresholds than could be obtained with resister-transistor circuits--the first popular discrete logic that was integrated. Therefore, it is not surprising that soon after the introduction of RTL, around 1960, integrated circuit manufacturers began translating discrete DTL into integrated devices also.

The basic DTL circuit is shown in Figure 1. Note that it requires two power supplies--a positive supply and a negative supply which is used to improve the turn-off time of the output inverter. Although the circuit would operate with only one supply, an undesirable compromise in the design would be necessitated to provide fairly symmetrical turn-on and turn-off times.

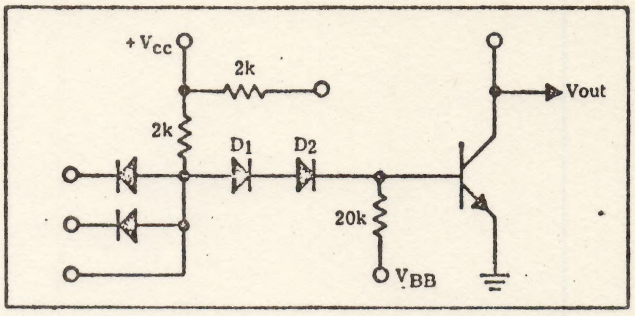

FIGURE 1 – BASIC DTL GATE CIRCUIT

If a single power supply were used, the charge could be pulled out of the base of the inverter when the input goes to a low logic state, allowing the inverter to turn-off, by either putting a small resistor between base and emitter or by making diodes D_1 and D_2 special slow recovery diodes. In integrated circuits, special purpose diodes are not desirable because they result in a lower yield item and, consequently, higher cost. On the other hand, a small resistor between base-emitter would limit the amount of base current to the inverter, thus reducing fan-out of the circuit. This fan-out could be improved by decreasing the size of the input pull-up resistor to supply the needed drive current. However, to do so would increase the power dissipated by the circuit as well as the current from each load circuit.

So in the basic DTL circuit, a negative power supply is used to turn off the output inverter, even though this second supply introduces additional complexity into the system.

DTL's advantages include large logic swings and high noise immunities. Input signal line noise margins run typically in excess of 1 volt. DTL can be classified in the medium speed range with circuit delay times from 30 to 70 ns. The binary element is capable of clocking rates in the 10 MHz range.

To summarize the performance of DTL vs other common logic forms, the chart (Figure 8) on the final page is presented. In this chart a comparison is shown of speed, power, noise, as well as other characteristics for DTL, RTL, variable threshold logic (VTL), current mode or emitter-coupled logic (ECL), and transistor-transistor logic (T^2L). This chart may help to put in the proper perspective some of the foregoing and following material.

THE MODIFIED DTL CIRCUIT

The need for a dual power supply, a feature adding considerable complexity to typical applications, has been eliminated in Motorola's version of DTL, called MDTL circuitry. The basic gate circuit of the MDTL family is shown in Figure 2. The circuit features an input transistor in place of one of the input offset diodes in conventional DTL. This is a stage of amplification that supplies turn-on drive to the output inverter. This source of current in the base allows for potential increase in fan-out with the MDTL design. It also means a much smaller base-emitter resistor can be used, and, consequently, a negative power supply is not required for rapid transistor turn-off. Further advantages of this approach are greater tolerances on resistor values, and relaxed gain specification on the inverter stage.

Circuit diagrams external to Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information in this Application Note has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

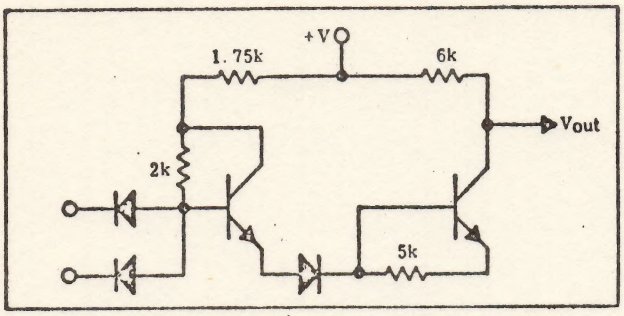

FIGURE 2 – BASIC MDTL GATE CIRCUIT

From a consideration of the design requirements for the MDTL circuit, it is apparent that less demand is made on resistor tolerances, h_{FE}, fan-out, and power dissipation than in the conventional DTL circuit. Therefore, although the performance characteristics of DTL and MDTL circuits are similar, the latter offers many advantages over DTL such as:

Single power supply operation.

Lower power dissipation--typically 8 mW per single gate for a 5V supply.

Larger drive capability--fan-out of 8 for a gate; 25 for the buffer.

Higher speed operation--20 to 50 ns typical propagation delay.

Better noise immunity--typically 1.2V at 25°C with worst case dc noise immunity specified at 350 mV over the full temperature range (-55° to 125°C) with maximum fan-out.

The transfer characteristic of a typical MDTL gate is given in Figure 3. V_{IL} is the minimum low threshold on the input, while V_{IH} is the maximum high threshold on the input. The worst case specified noise margins with a

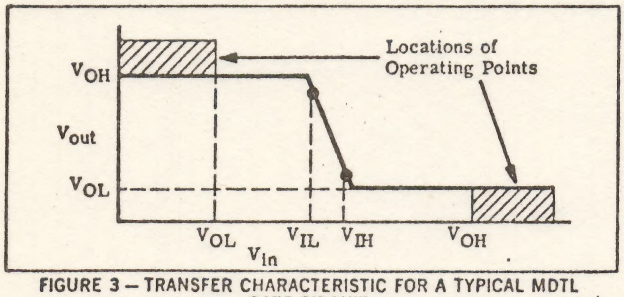

FIGURE 3 – TRANSFER CHARACTERISTIC FOR A TYPICAL MDTL GATE CIRCUIT

low level input and a high level input are $V_{IL} - V_{OL}$ and $V_{OH} - V_{IH}$ respectively. The low level noise margin will always be in excess of 350 mV while the high level noise margin will be greater than 400 mV over the full temperature range of -55° to 125°C.

Increased noise margins are obtained when circuits are not fully loaded. Worst case noise thresholds generally are better than 600 mV in systems that do not employ the maximum drive capability of each circuit.

The circuits discussed thus far have thresholds that are appreciable. These circuits can generally be considered to be insensitive to noise inputs on any line up to 500 millivolts. However, if the noise level is high enough, these circuits will be disturbed. Depending upon the environment, noise may or may not be a serious problem, but along with proper grounding techniques, noise problems should be considered from the very beginning of a design.

HIGH NOISE IMMUNITY DTL

Some applications require better noise immunity than that available from standard DTL or any of the other IC logic lines commonly used today. For this reason, Motorola further modified the basic DTL circuit to improve noise margins. This modified DTL type circuitry is called Variable Threshold Logic (MVTL) circuitry.

In many applications, integrated circuits must operate close to solenoids, relays, and high-voltage testing devices that create noise spikes far in excess of the noise immunity levels of conventional logic gates. At first, engineers had to resort to bulky packaging and shielding that was not always completely effective, but, now, MVTL circuitry often provides adequate noise immunity without resorting to these shielding techniques.

MVTL elements are particularly useful in systems that have external noise sources generating large voltage disturbances on signal and ground lines. High noise rejection at the input allows these circuits to operate reliably where signal paths run close to units that supply large output voltages or where high voltage lines must be interrupted.

The basic MVTL gate circuit is shown in Figure 4. This circuit differs from the conventional DTL gate in that one of the input offset diodes has been replaced by a voltage dropping resistor. Also, a current source transistor, Q_1, is used, whereas in DTL there is a pull-down resistor in the base of the output inverter. A brief look at the circuit operation will explain how these changes provide additional noise immunity.

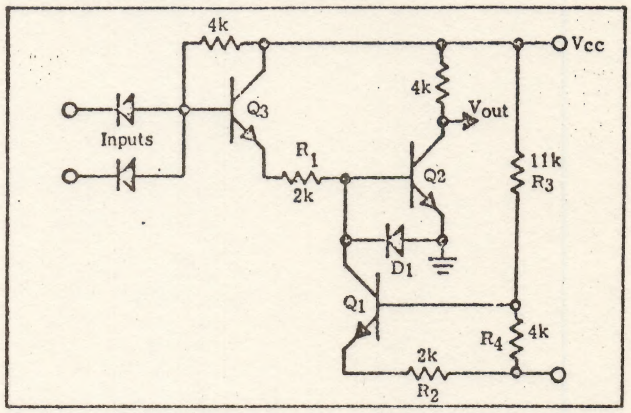

FIGURE 4 – BASIC MVTL GATE CIRCUIT

The amount of current that flows through the current source transistor Q_1 is determined by the power supply levels and the ratio R_3/R_4. Transistor Q_1 in turn provides a current through the offset resistor R_1, and it is the resultant voltage drop across this resistor that determines the input threshold of the circuit. Thus, due to the circuit action described above, the input threshold can be controlled over a 2 to 5 volt range simply by changing the values of V_{CC} and V_{EE}. In order to maintain similar noise immunities for high and low logic levels, the V_{CC} and V_{EE} supplies are made equal.

For $V_{CC} = V_{EE} = 4V$, the input threshold is 2V. If the supply voltages are increased to 10V, the threshold increases to 5V. A good approximation for noise immunity is one-half the V_{CC} supply voltage, although noise margins are slightly less than these values due to output saturation voltages, input leakages, and finite output transition widths.

To obtain various performance characteristics, the ratio V_{EE}/V_{CC} may be changed. For instance, while

maintaining a constant V_{CC}, V_{EE} may be varied to obtain changes in input and ground line noise immunities, circuit speed, fan-out, and power dissipation.

The gate voltage transfer characteristic plotting V_{OUT} vs. V_{IN} for a typical gate circuit helps explain the noise rejection capabilities of MVTL and is shown in Figure 5. From the characteristic curve, we see that the input logic "0" dc noise margin ($\Delta 0$) is equal to the difference between the input voltage required to make the output inverter conduct (V_0) and the low level at the input (V_{CES}). The input logic "1" dc noise margin ($\Delta 1$) is equal to the difference between the high input level (V_{CC}) and the input voltage at which the inverter starts to come out of saturation (V_1). A change of slope occurs in the active region at $V_{IN} = V'$. This is the point at which the load diodes turn on and the voltage gain of the output stage decreases.

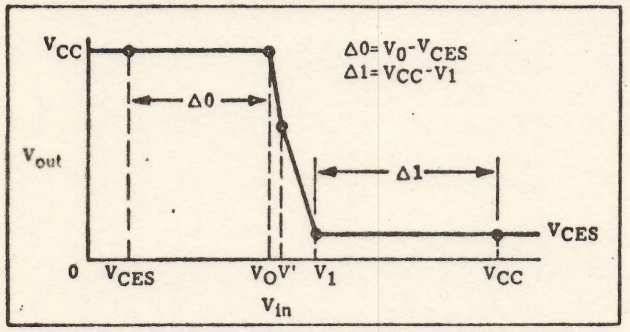

FIGURE 5 – TRANSFER CHARACTERISTIC FOR A TYPICAL MVTL GATE CIRCUIT

MVTL was designed to have a constant value of noise immunity over the temperature range. This is illustrated in Figure 6 which shows a comparison of the DTL and VTL transfer characteristics. Here it should be noted that the threshold of VTL remains essentially constant over temperature.

Ground noise rejection capability is another important feature of this logic family. While not as high as input noise margins, the ground noise margin is considerable, and has a large margin of superiority over presently available integrated logic lines. At 10V operation, MVTL circuits exhibit a typical dc ground line noise immunity of 3.7V. Figure 7 shows how additional ground noise immunity is obtainable by adjusting the V_{EE} bias below the value of V_{CC}. While keeping V_{CC} at 10V, practically 400 mV of ground noise immunity can be added by reducing the V_{EE} supply from -10V to about -8V. Notice that while reducing the ratio V_{EE}/V_{CC} improves the ground noise condition, a certain loss does occur in the input logic "0" dc noise margin. At the same time, however, power is reduced while circuit speed and fan-out improve.

The power consumed by a single gate circuit will vary from 82 mW with 10V supplies to 12 mW with 4V supplies. Typical propagation delay of the MVTL gate will vary from 60 ns with 4V supplies to 48 ns with 10V supplies at 25°C. Thus, the speed, power dissipation, and noise immunity of the MVTL circuits are quite flexible, and the designer is free to select his own operating conditions to satisfy his circuit needs.

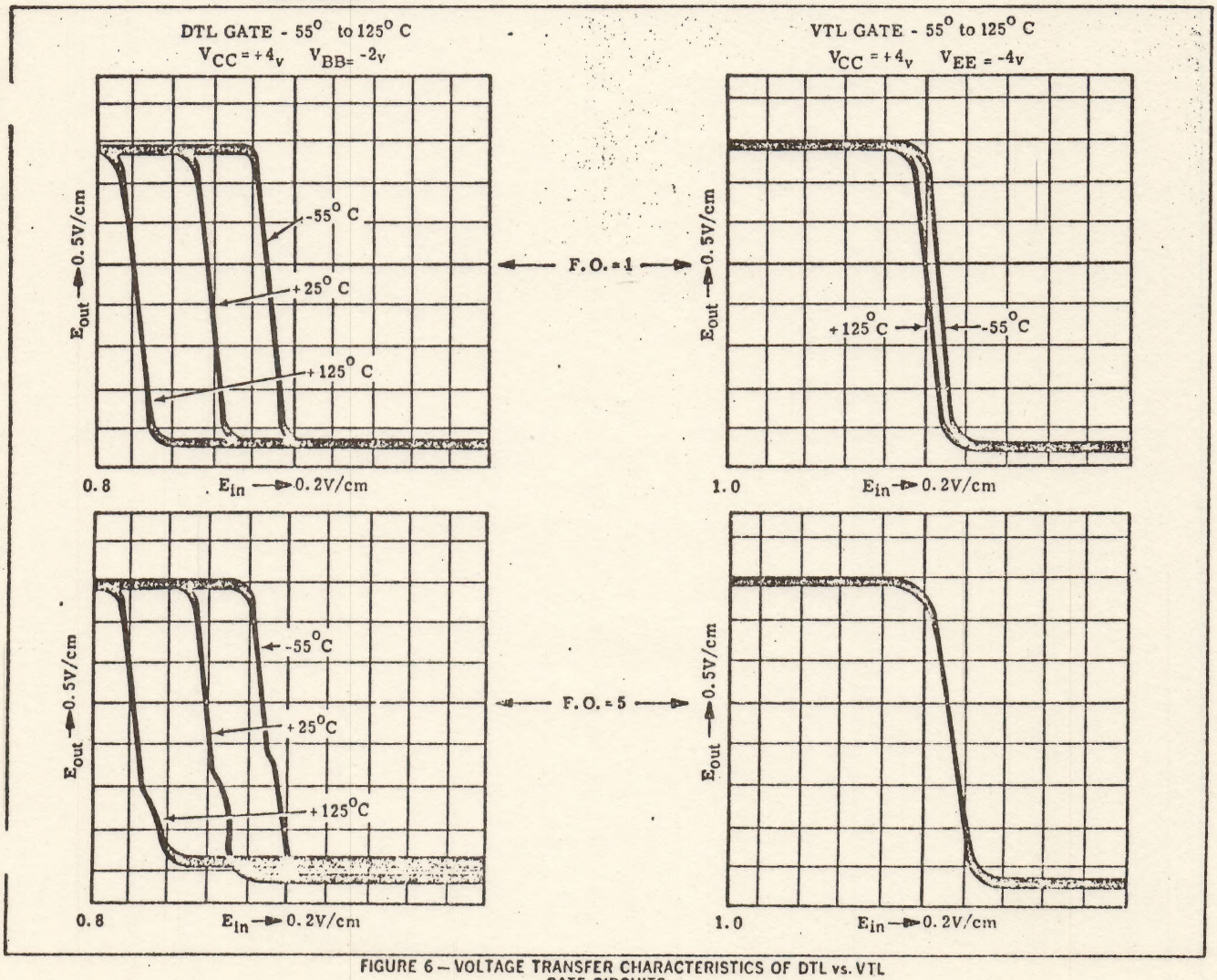

FIGURE 6 – VOLTAGE TRANSFER CHARACTERISTICS OF DTL vs. VTL GATE CIRCUITS

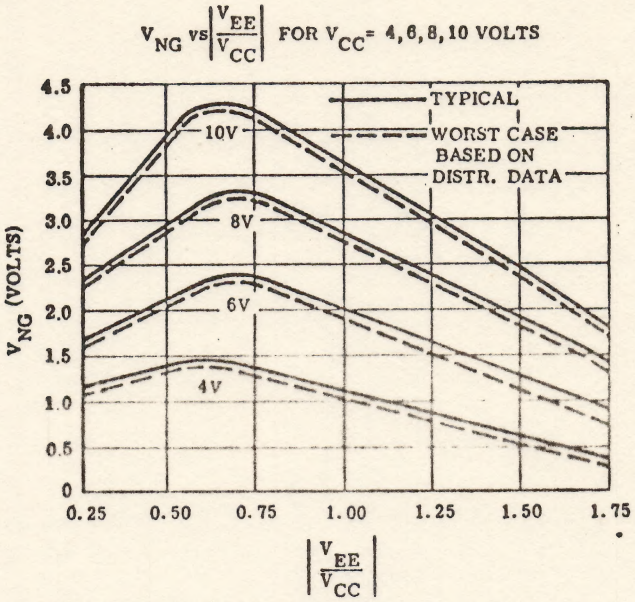

FIGURE 7 — MVTL GROUND NOISE IMMUNITY CAN BE OPTIMIZED BY SETTING THE V_u/V_{cc} RATIO AT APPROXIMATELY 0.6

MVTL circuits have been designed primarily for industrial applications and therefore their characteristics are specified for the 0° to 75°C temperature range. Noise margins will remain essentially constant over the operational temperature range. This is another significant advantage over other logic lines. For example, the threshold point for DTL circuits will change at the rate of about 3.5 mV per °C of temperature variation.

A fan-out of five is the maximum specified for MVTL. These devices may be used with a larger number of load circuits than five, but with the penalty of some loss in noise margin.

CONCLUSION

This note has presented some of the considerations a user should make prior to using DTL integrated circuits. It has been pointed out that DTL IC's rank high as far as immunity to extraneous noise signals is concerned. Its speed is in the 5 to 10 MHz range, comparable to the high speed RTL circuitry but well below the capability of ECL and T^2L circuits. If noise is a particular concern, there is available a special version of DTL, called VTL, which has been designed specifically to combat noise problems.

Logic	Form	Avg. Prop. Delay Time (ns)	Binary Element Clock Freq. (MHz)	Gate Power Diss. (mW)	Internal Noise Margin	External Noise Margin	Gate Fan-Out	Temperature Range	Power Supply Voltage or Signal Voltage
MRTL*	Resistor-Transistor	24	8 (min.)	12	Fair	Fair	5	15-55°C 0-100°C —55-125°C	3.0 ± 10% 3.6 ± 10%
mW MRTL	Resistor-Transistor	45	1-3	2.5	Fair	Fair	5	15-55°C —55-125°C	3.0 ± 10% 3.6 ± 10%
DTL	Diode-Transistor	30	10	9	Fair	Good	5	0-75°C —55-125°C	$^{4.0}_{-2.0}$ ± 10%
MDTL	Diode-Transistor	30	12	8	Fair	Good	8	0-75°C —55-125°C	5.0 ± 10%
MVTL	Diode-Transistor	50-60	1	12-80	Good	Excellent	5	0-75°C	±4 to ±10
MECL	Current mode	6	30	35	Excellent	Fair	25	0-75°C —55-125°C	5.2 ± 20%
MT^2L	Transistor-Transistor	10	20	15	Good	Good	12 or 6 15 or 7	0-75°C —55-125°C	5.0 ± 10%

FIGURE 8